

S/N Unknown

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble et al.

Examiner: Unknown

Serial No.: Unknown

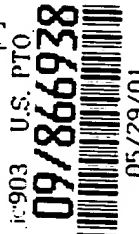
Group Art Unit: Unknown

Filed: Herewith

Docket: 303.330US3

Title: ULTRA HIGH DENSITY FLASH MEMORY

PATENT



INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for review in connection with the above-identified patent application. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner be returned to the Applicants.

In accordance with 37 C.F.R. § 1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicants' prior U.S. application, Serial No. 09/035,304, filed on February 27, 1998, which is relied upon for an earlier filing date under 35 U.S.C. § 120.

Applicants respectfully request consideration of these references during prosecution of the above-identified matter. The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

WENDELL P. NOBLE ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
(612) 373-6913

Date

5/29/2001

By

Edward J. Brooks, III

Edward J. Brooks, III  
Reg. No. 40,925

"Express Mail" mailing label number: EL671639402US

Date of Deposit: May 29, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Form 1449*	Atty. Docket No.: 303.330US3	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Wendell P. Noble et al.	
	Filing Date: Herewith	Group: Unknown

## U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	3,657,575	04/18/1972	Taniguchi, K., et al.	307	304	03/15/71
	3,806,741	04/23/1974	Smith	307	304	05/17/72
	4,051,354	09/27/1977	Choate, W.C.	235	312	07/03/75
	4,604,162	08/05/1986	Sobczak, Z.P.	156	657	12/23/85
	4,920,065	04/24/1990	Chin, D., et al.	437	52	10/27/89
	4,958,318	09/18/1990	Harari, E.	365	149	07/08/88
	4,987,089	01/22/1991	Roberts	437	34	07/23/90
	5,006,909	04/09/1991	Kosa, Y.	357	23.6	10/30/89
	5,017,504	05/21/1991	Nishimura, et al.	437	40	04/21/89
	5,021,355	06/04/1991	Dhong, et al.	437	35	05/18/90
	5,028,977	07/02/1991	Kenneth, et al.	357	43	06/16/89
	5,057,896	10/01/1991	Gotou, H.	357	49	05/30/89
	5,072,269	12/10/1991	Hieda, K.	357	23.6	03/15/89
	5,110,752	05/05/1992	Lu	437	47	07/10/91
	5,128,831	07/07/1992	Fox, III, A.C., et al.	361	396	10/31/91
	5,156,987	10/20/1992	Sandhu, et al.	437	40	12/18/91
	5,177,576	01/05/1993	Kimura, S., et al.	257	71	05/06/91
	5,202,278	04/13/1993	Mathews, et al.	437	47	09/10/91
	5,216,266	06/01/1993	Ozaki, H.	257	302	04/09/91
	5,223,081	06/29/1993	Doan	156	628	07/03/91
	5,266,514	11/30/1993	Tuan, H., et al.	437	52	12/21/92
	5,292,676	03/08/1994	Manning	437	46	07/29/92
	5,316,962	05/31/1994	Matsuo, N., et al.	437	52	08/06/92
	5,320,880	06/14/1994	Sandhu, G.S., et al.	427	578	11/18/93
	5,385,854	01/31/1995	Batra, et al.	437	41	07/15/93
	5,392,245	02/21/1995	Manning	365	200	08/13/93
	5,409,563	04/25/1995	Cathey	156	643	02/26/93
	5,414,287	05/09/1995	Hong, G.	257	316	04/25/94
	5,427,972	06/27/1995	Shimizu, M., et al.	437	52	04/18/90
	5,432,739	07/11/1995	Pein, H.B.	365	185	06/17/94
	5,445,986	08/29/1995	Hirota, T.	437	60	09/01/94
	5,451,889	09/19/1995	Heim, B.B., et al.	326	81	03/14/94
	5,460,988	10/24/1995	Hong, G.	437	43	04/25/94
	5,483,094	01/09/1996	Sharma, U., et al.	257	316	09/26/94
	5,495,441	02/27/1996	Hong, G.	365	185.01	05/18/94
	5,502,629	03/26/1996	Ito, H., et al.	363	60	03/28/95
	5,508,542	04/16/1996	Geiss, et al.	257	301	10/28/94
	5,519,236	05/21/1996	Ozaki, T.	257	302	06/27/94
	5,563,083	10/08/1996	Pein, H.B.	437	43	04/21/95
	5,574,299	11/12/1996	Kim, H.	257	296	06/29/95
	5,616,934	04/01/1997	Dennison, et al.	257	67	03/22/96

Examiner	Date Considered
----------	-----------------

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

903 U.S. PTO  
09/866938  
05/29/01

Form 1449*	Atty. Docket No.: 303.330US3	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Wendell P. Noble et al.	
	Filing Date: Herewith	Group: Unknown

## U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	5,640,342	06/17/1997	Gonzalez	365	156	11/20/95
	5,641,545	06/24/1997	Sandhu, G.S.	427	573	06/07/95
	5,644,540	07/01/1997	Manning	365	200	02/17/95
	5,646,900	07/08/1997	Tsukude, et al.	365	205	01/11/96
	5,691,230	11/25/1997	Forbes, L.	437	62	09/04/96
	5,705,415	01/06/1998	Orlowski, M.K., et al.	437	43	10/04/94
	5,789,967	08/04/1998	Kato, Y.	327	408	04/01/96
	5,821,796	10/13/1998	Yaklin, D., et al.	327	313	09/23/96
	5,852,375	12/22/1998	Byrne, T.G., et al.	327	108	02/07/97
	5,909,618	06/01/1999	Forbes, L., et al.	438	242	07/08/97
	5,914,511	06/22/1999	Noble, W.P., et al.	257	302	10/06/97

## FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes   No
	63-066963	03/25/1988	Japan	H01L	27/10	

## OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
	Asai, S., et al., "Technology Challenges for Integration Near and Below 0.1 micrometer", <u>Proceedings of the IEEE</u> , 85(4), Special Issue on Nanometer-Scale Science & Technology, 505-520, (Apr. 1997)
	Askin, H.O., et al., "Fet Device Parameters Compensation Circuit", <u>IBM Technical Disclosure Bulletin</u> , 14, 2088-2089, (December 1971)
	Blalock, T.N., et al., "A High-Speed Sensing Scheme for 1T Dynamic RAM's Utilizing the Clamped Bit-Line Sense Amplifier", <u>IEEE Journal of Solid-State Circuits</u> , 27(4), pp. 618-624, (April 1992)
	Bomchil, G., et al., "Porous Silicon: The Material and its Applications in Silicon-On-Insulator Technologies", <u>Applied Surface Science</u> , 41/42, 604-613, (1989)
	Burnett, D., et al., "Implications of Fundamental Threshold Voltage Variations for High-Density SRAM and Logic Circuits", <u>1994 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 15-16, (June 1994)
	Burnett, D., et al., "Statistical Threshold-Voltage Variation and its Impact on Supply-Voltage Scaling", <u>Proceedings SPIE: Microelectronic Device and Multilevel Interconnection Technology</u> , 2636, 83-90, (1995)

Examiner	Date Considered
----------	-----------------

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.330US3	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Wendell P. Noble et al.	
	Filing Date: Herewith	Group: Unknown

## OTHER DOCUMENTS

\*\*Examiner  
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Chen, M., et al., "Back-Gate Forward Bias Method for Low Voltage CMOS Digital Cicuits", <u>IEEE Transactions on Electron Devices</u> , 43, 904-909, (1996)
	Clemen, R., et al., "VT-compensated TTL-Compatible Mos Amplifier", <u>IBM Technical Disclosure Bulletin</u> , 21, 2874-2875, (1978)
	De, V.K., et al., "Random MOSFET Parameter Fluctuation Limits to Gigascale Integration (GSI)", <u>1996 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 198-199, (June 11-13, 1996)
	De, V.K., et al., "Random Mosfet Parameter Fluctuation Limits to Gigascale Integration (GST)", <u>Symposium on VLSI Technology Digest of Technical Papers</u> , 198-199, (1996)
	DeBar, D.E., "Dynamic Substrate Bias to Achieve Radiation Hardening", <u>IBM Technical Disclosure Bulletin</u> , 25, 5829-5830, (1983)
	Fong, Y., et al., "Oxides Grown on Textured Single-Crystal Silicon--Dependence on Process and Application in EEPROMs", <u>IEEE Transactions on Electron Devices</u> , 37(3), pp. 583-590, (March 1990)
	Forbes, L., "Automatic On-clip Threshold Voltage Compensation", <u>IBM Technical Disclosure Bulletin</u> , 14, 2894-2895, (1972)
	Forbes, L., et al., "Resonant Forward-Biased Guard-Ring Diodes for Suppression of Substrate Noise in Mixed-Mode CMOS Circuits", <u>Electronics Letters</u> , 31, 720-721, (April 1995)
	Foster, R., et al., "High Rate Low-Temperature Selective Tungsten", <u>In: Tungsten and Other Refractory Metals for VLSI Applications III</u> , V.A. Wells, ed., Materials Res. Soc., Pittsburgh, PA, 69-72, (1988)
	Frantz, H., et al., "Mosfet Substrate Bias-Voltage Generator", <u>IBM Technical Disclosure Bulletin</u> , 11, 1219-1220, (March 1969)
	Fuse, T., et al., "A 0.5V 200MHz 1-Stage 32b ALU Using a Body Bias Controlled SOI Pass-Gate Logic", <u>1997 IEEE International Solid-State Circuits Conference, Digest of Technical Papers</u> , 286-287, (1997)
	Gong, S., et al., "Techniques for Reducing Switching Noise in High Speed Digital Systems", <u>Proceedings of the 8th Annual IEEE International ASIC Conference and Exhibit</u> , Austin, TX, 21-24, (1995)

Examiner	Date Considered
----------	-----------------

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.330US3	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Wendell P. Noble et al.	
	Filing Date: Herewith	Group: Unknown

## OTHER DOCUMENTS

\*\*Examiner  
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Hao, M.Y., et al., "Electrical Characteristics of Oxynitrides Grown on Textured Single-Crystal Silicon", <u>Appl. Phys. Lett.</u> , 60, 445-447, (Jan. 1992)
	Harada, M., et al., "Suppression of Threshold Voltage Variation in MTCMOS/SIMOX Circuit Operating Below 0.5 V", <u>1996 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 96-97, (June 11-13, 1996)
	Heavens, O., <u>Optical Properties of Thin Solid Films</u> , Dover Pubs. Inc., New York, 155-206, (1965)
	Horie, H., et al., "Novel High Aspect Ratio Aluminum Plug for Logic/DRAM LSI's Using Polysilicon-Aluminum Substitute", <u>Technical Digest: IEEE International Electron Devices Meeting</u> , San Francisco, CA, 946-948, (1996)
	Jun, Y.K., et al., "The Fabrication and Electrical Properties of Modulated Stacked Capacitor for Advanced DRAM Applications", <u>IEEE Electron Device Letters</u> , 13, 430-432, (Aug. 1992)
	Jung, T.S., et al., "A 117-mm <sup>2</sup> 3.3-V Only 128-Mb Multilevel NAND Flash Memory for Mass Storage Applications", <u>IEEE Journal of Solid-State Circuits</u> , 31, 1575-1583, (Nov. 1996)
	Kim, Y.S., et al., "A Study on Pyrolysis DMEAA for Selective Deposition of Aluminum", In: <u>Advanced Metallization and Interconnect Systems for ULSI Applications in 1995</u> , R.C. Ellwanger, et al., (eds.), Materials Research Society, Pittsburgh, PA, 675-680, (1996)
	Klaus, et al., "Atomic Layer Controlled Growth of SiO <sub>2</sub> Films Using Binary Reaction Sequence Chemistry", <u>Applied Physics Lett.</u> 70(9), 1092-94, (3 March 1997)
	Koshida, N., et al., "Efficient Visible Photoluminescence from Porous Silicon", <u>Japanese Journal of Applied Physics</u> , 30, L1221- L1223, (July 1991)
	Lehmann, et al., "A Novel Capacitor Technology Based on Porous Silicon", <u>Thin Solid Films</u> 276, Elsevier Science, 138-42, (1996)
	Lehmann, V., "The Physics of Macropore Formation in Low Doped n-Type Silicon", <u>Journal of the Electrochemical Society</u> , 140(10), 2836-2843, (Oct. 1993)

Examiner	Date Considered
----------	-----------------

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.330US3	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Wendell P. Noble et al.	
	Filing Date: Herewith	Group: Unknown

## OTHER DOCUMENTS

\*\*Examiner  
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Masu, K., et al., "Multilevel Metallization Based on Al CVD", <u>1996 IEEE Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 44-45, (June 11-13, 1996)
	McCredie, B.D., et al., "Modeling, Measurement, and Simulation of Simultaneous Switching Noise", <u>IEEE Transactions on Components, Packaging, and Manufacturing Technology -- Part B</u> , 19, 461-472, (Aug. 1996)
	Muller, K., et al., "Trench Storage Node Technology for Gigabit DRAM Generations", <u>Digest IEEE International Electron Devices Meeting</u> , San Francisco, CA, 507-510, (Dec. 1996)
	Ohba, T., et al., "Evaluation on Selective Deposition of CVD W Films by Measurement of Surface Temperature", <u>In: Tungsten and Other Refractory Metals for VLSI Applications II</u> , Materials Research Society, Pittsburgh, PA, 59-66, (1987)
	Ohba, T., et al., "Selective Chemical Vapor Deposition of Tungsten Using Silane and Polysilane Reductions", <u>In: Tungsten and Other Refractory Metals for VLSI Applications IV</u> , Materials Research Society, Pittsburgh, PA, 17-25, (1989)
	Ott, A.W., et al., "Al3O3 Thin Film Growth on Si(100) Using Binary Reaction Sequence Chemistry", <u>Thin Solid Films</u> , Vol. 292, 135-44, (1997)
	Pein, H., et al., "A 3-D Sidewall Flash EPROM Cell and Memory Array", <u>IEEE Transactions on Electron Devices</u> , 40, 2126-2127, (Nov. 1993)
	Pein, H., et al., "Performance of the 3-D PENCIL Flash EPROM Cell and Memory Array", <u>IEEE Transactions on Electron Devices</u> , 42, 1982-1991, (November, 1995)
	Pein, H.B., et al., "Performance of the 3-D Sidewall Flash EPROM Cell", <u>IEEE International Electron Devices Meeting, Technical Digest</u> , 11-14, (1993)
	Puri, Y., "Substrate Voltage Bounce in NMOS Self-biased Substrates", <u>IEEE Journal of Solid-State Circuits</u> , SC-13, 515-519, (August 1978)
	Ramo, S., et al., <u>Fields and Waves in Communication Electronics, Third Edition</u> , John Wiley & Sons, Inc., pp. 428-433, (1994)

Examiner	Date Considered
----------	-----------------

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.330US3	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Wendell P. Noble et al.	
	Filing Date: Herewith	Group: Unknown

## OTHER DOCUMENTS

\*\*Examiner  
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Sagara, K., et al., "A 0.72 micro-meter <sup>2</sup> Recessed STC (RSTC) Technology for 256Mbit DRAMs using Quarter-Micron Phase-Shift Lithography", <u>1992 Symposium on VLSI Technology, Digest of Technical Papers</u> , Seattle, WA, 10-11, (June 2-4, 1992)
	Saito, M., et al., "Technique for Controlling Effective V <sub>th</sub> in Multi-Gbit DRAM Sense Amplifier", <u>1996 Symposium on VLSI Circuits, Digest of Technical Papers</u> , Honolulu, HI, 106-107, (June 13-15, 1996)
	Seevinck, E., et al., "Current-Mode Techniques for High-Speed VLSI Circuits with Application to Current Sense Amplifier for CMOS SRAM's", <u>IEEE Journal of Solid State Circuits</u> , 26(4), pp. 525-536, (April 1991)
	Senthinathan, R., et al., "Reference Plane Parasitics Modeling and Their Contribution to the Power and Ground Path "Effective" Inductance as Seen by the Output Drivers", <u>IEEE Transactions on Microwave Theory and Techniques</u> , 42, 1765-1773, (Sep. 1994)
	Sherony, M.J., et al., "Reduction of Threshold Voltage Sensitivity in SOI MOSFET's", <u>IEEE Electron Device Letters</u> , 16, 100-102, (Mar. 1995)
	Shimomura, K., et al., "A 1V 46ns 16Mb SOI-DRAM with Body Control Technique", <u>1997 IEEE International Solid-State Circuits Conference, Digest of Technical Papers</u> , 68-69, (Feb. 6, 1997)
	Stanisic, B.R., et al., "Addressing Noise Decoupling in Mixed-Signal IC's: Power Distribution Design and Cell Customization", <u>IEEE Journal of Solid-State Circuits</u> , 30, 321-326, (Mar. 1995)
	Stellwag, T.B., et al., "A Vertically-Integrated GaAs Bipolar DRAM Cell", <u>IEEE Transactions on Electron Devices</u> , 38, 2704-2705, (Dec. 1991)
	Su, D.K., et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", <u>IEEE Journal of Solid-State Circuits</u> , 28(4), 420-430, (Apr. 1993)
	Suntola, T., "Atomic Layer Epitaxy", <u>Handbook of Crystal Growth 3, Thin Films of Epitaxy, Part B: Growth Mechanics and Dynamics</u> , Elsevier, Amsterdam, 601-63, (1994)
	Sze, S.M., <u>VLSI Technology</u> , 2nd Edition, Mc Graw-Hill, NY, 90, (1988)

Examiner	Date Considered
----------	-----------------

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.330US3	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Wendell P. Noble et al.	
	Filing Date: Herewith	Group: Unknown

## OTHER DOCUMENTS

\*\*Examiner  
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Takato, H., et al., "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", <u>IEEE International Electron Devices Meeting, Technical Digest</u> , 222-225, (1988)
	Temmler, D., "Multilayer Vertical Stacked Capacitors (MVSTC) for 64Mbit and 256Mbit DRAMs", <u>1991 Symposium on VLSI Technology, Digest of Technical Papers</u> , Oiso, 13-14, (May 28-30, 1991)
	Vittal, A., et al., "Clock Skew Optimization for Ground Bounce Control", <u>1996 IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers</u> , San Jose, CA, 395-399, (Nov. 10-14, 1996)
	Wang, P.W., et al., "Excellent Emission Characteristics of Tunneling Oxides Formed Using Ultrathin Silicon Films for Flash Memory Devices", <u>Japanese Journal of Applied Physics</u> , 35, 3369-3373, (June 1996)
	Watanabe, H., et al., "A Novel Stacked Capacitor with Porous-Si Electrodes for High Density DRAMs", <u>1993 Symposium on VLSI Technology, Digest of Technical Papers</u> , Kyoto, Japan, 17-18, (1993)
	Watanabe, H., et al., "An Advanced Fabrication Technology of Hemispherical Grained (HSG) Poly-Si for High Capacitance Storage Electrodes", <u>Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials</u> , Yokohama, Japan, 478-480, (1991)
	Watanabe, H., et al., "Device Application and Structure Observation for Hemispherical-Grained Si", <u>J. Appl. Phys.</u> , 71, 3538-3543, (Apr. 1992)
	Watanabe, H., et al., "Hemispherical Grained Silicon (HSG-Si) Formation on In-Situ Phosphorous Doped Amorphous-Si Using the Seeding Method", <u>Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials</u> , Tsukuba, Japan, 422-424, (1992)
	Wooley, et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed Signal Integrated Circuits", <u>IEEE Journal of Solid State Circuits</u> , Vol SC-28, 420-30, (1993)
	Yoshikawa, K., "Impact of Cell Threshold Voltage Distribution in the Array of Flash Memories on Scaled and Multilevel Flash Cell Design", <u>1996 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 240-241, (June 11-13, 1996)

Examiner

Date Considered

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.